a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

2. (Unchanged) The computer system of claim 1, wherein the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a normal mode and a low power mode.

3. (Unchanged) The computer system of claim 2, wherein the refresh timing circuit further comprises:

a clock generator for generating the clock pulses;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

4. (Unchanged) The computer system of claim 3, wherein the first counter counts the number of clock pulses generated by the clock generator.

5. (Unchanged) The computer system of claim 4, wherein the first counter transmits data to the storage register whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a prior memory refresh event.

6. (Unchanged) The computer system of claim 5, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

7. (Unchanged) The computer system of claim 6, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

8. (Unchanged) The computer system of claim 7, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

9. (Unchanged) The computer system of claim 4, wherein the refresh timing circuit further comprises a second counter.

10. (Unchanged) The computer system of claim 9, wherein the first counter counts the number of clock pulses generated by the clock generator while the computer system is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the computer system is operating in a normal mode.

11. (Unchanged) The computer system of claim 10, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

12. (Unchanged) The computer system of claim 11, wherein the second counter is deactivated and the first counter is activated whenever the computer system transitions from the normal mode to the low power mode.

13. (Unchanged) The computer system of claim 12, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

14. (Unchanged) The computer system of claim 3, wherein the refresh timing circuit includes a second counter for triggering memory refresh events whenever the computer system is operating in the normal mode

15. (Unchanged) The computer system of claim 1, wherein the memory is an Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller is an EDO DRAM controller.

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16. (Amended) A memory controller comprising:

a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

17. (Amended) The memory controller of claim 16, wherein the refresh timing circuit further comprises:

a clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

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a comparator coupled to the clock generator, the counter and the storage register.

18. (Amended) The memory controller of claim 17, wherein the memory controller operates in a normal mode and a low power mode.

19. (Amended) The memory controller of claim 18, wherein the first counter counts the number of clock pulses generated by the clock generator.

20. (Amended) The memory controller of claim 19, wherein the first counter transmits data to the storage register whenever the memory controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

21. (Amended) The memory controller of claim 20, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

22. (Amended) The memory controller of claim 21, wherein the first counter transmits signals to the comparator whenever the memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

23. (Amended) The memory controller of claim 22, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

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24. (Amended) The memory controller of claim 19, wherein the refresh timing circuit further comprises a second counter.

25. (Amended) The memory controller of claim 24, wherein the first counter counts the number of clock pulses generated by the clock generator while the memory controller is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the memory controller is operating in the normal mode.

26. (Amended) The memory controller of claim 25, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the memory controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

27. (Amended) The memory controller of claim 26, wherein the second counter is deactivated and the first counter is activated whenever the memory controller transitions from the normal mode to the low power mode.

28. (Amended) The memory controller of claim 27, wherein the first counter transmits signals to the comparator whenever the memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

**Please add the following new claims:**

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38. (New) A refresh timing circuit comprising:

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an internal clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

39. (New) The refresh timing circuit of claim 38, wherein the refresh timing circuit operates in a normal mode and a low power mode.

40. (New) The refresh timing circuit of claim 39, wherein the first counter counts the number of clock pulses generated by the clock generator.

41. (New) The refresh timing circuit of claim 40, wherein the first counter transmits data to the storage register whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

42. (New) The refresh timing circuit of claim 41, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

43. (New) The refresh timing circuit of claim 42, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

44. (New) The refresh timing circuit of claim 43, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

45. (New) The refresh timing circuit of claim 40, further comprising a second counter.

46. (New) The refresh timing circuit of claim 45, wherein the first counter counts the number of clock pulses generated by the clock generator while the refresh timing circuit is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the refresh timing circuit is operating in the normal mode.

47. (New) The refresh timing circuit of claim 46, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

48. (New) The refresh timing circuit of claim 47, wherein the second counter is deactivated and the first counter is activated whenever the refresh timing circuit transitions from the normal mode to the low power mode.

49. (New) The refresh timing circuit of claim 48, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low

power mode, the signal representing the number of clock pulses received from the clock generator.